



INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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<p>(21) International Application Number: PCT/US99/26483</p> <p>(22) International Filing Date: 9 November 1999 (09.11.99)</p> <p>(30) Priority Data:</p> <table> <tr> <td>60/107,877</td> <td>9 November 1998 (09.11.98)</td> <td>US</td> </tr> <tr> <td>60/108,319</td> <td>13 November 1998 (13.11.98)</td> <td>US</td> </tr> <tr> <td>60/130,616</td> <td>22 April 1999 (22.04.99)</td> <td>US</td> </tr> </table> <p>(71) Applicant (<i>for all designated States except US</i>): BROADCOM CORPORATION [US/US]; 16215 Alton Parkway, Irvine, CA 92618 (US).</p> <p>(72) Inventor; and</p> <p>(75) Inventor/Applicant (<i>for US only</i>): HATAMIAN, Mehdi [US/US]; 25681 Pacific Hills, Mission Viejo, CA 92692 (US).</p> <p>(74) Agent: HOANG, Phuong-Quan; Christie, Parker & Hale, LLP, P.O. Box 7068, Pasadena, CA 91109-7068 (US).</p>		60/107,877	9 November 1998 (09.11.98)	US	60/108,319	13 November 1998 (13.11.98)	US	60/130,616	22 April 1999 (22.04.99)	US	<p>(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TI, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).</p> <p>Published <i>With international search report.</i></p> <p>(88) Date of publication of the international search report: 17 August 2000 (17.08.00)</p>	
60/107,877	9 November 1998 (09.11.98)	US										
60/108,319	13 November 1998 (13.11.98)	US										
60/130,616	22 April 1999 (22.04.99)	US										
<p>(54) Title: FIR FILTER STRUCTURE WITH LOW LATENCY FOR GIGABIT ETHERNET APPLICATIONS</p> <pre> graph LR x((x(n))) --> Z1[] Z1 --> M1(()) M1 --> S1(()) S1 --> Z2[] Z2 --> M2(()) M2 --> S2(()) S2 --> Z3[] Z3 --> M3(()) M3 --> S3(()) S3 --> Z4[] Z4 --> M4(()) M4 --> S4(()) S4 --> Z5[] Z5 --> M5(()) M5 --> S5(()) S5 --> Z6[] Z6 --> M6(()) M6 --> S6(()) S6 --> Z7[] Z7 --> M7(()) M7 --> S7(()) S7 --> Z8[] Z8 --> M8(()) M8 --> S8(()) S8 --> y((y(n))) S1 --> Z2 S2 --> Z3 S3 --> Z4 S4 --> Z5 S5 --> Z6 S6 --> Z7 S7 --> Z8 Z1 --> M1 Z2 --> M2 Z3 --> M3 Z4 --> M4 Z5 --> M5 Z6 --> M6 Z7 --> M7 Z8 --> M8 style Z1 fill:#fff,stroke:#000,stroke-width:1px style Z2 fill:#fff,stroke:#000,stroke-width:1px style Z3 fill:#fff,stroke:#000,stroke-width:1px style Z4 fill:#fff,stroke:#000,stroke-width:1px style Z5 fill:#fff,stroke:#000,stroke-width:1px style Z6 fill:#fff,stroke:#000,stroke-width:1px style Z7 fill:#fff,stroke:#000,stroke-width:1px style Z8 fill:#fff,stroke:#000,stroke-width:1px style M1 fill:#fff,stroke:#000,stroke-width:1px style M2 fill:#fff,stroke:#000,stroke-width:1px style M3 fill:#fff,stroke:#000,stroke-width:1px style M4 fill:#fff,stroke:#000,stroke-width:1px style M5 fill:#fff,stroke:#000,stroke-width:1px style M6 fill:#fff,stroke:#000,stroke-width:1px style M7 fill:#fff,stroke:#000,stroke-width:1px style M8 fill:#fff,stroke:#000,stroke-width:1px style S1 fill:#fff,stroke:#000,stroke-width:1px style S2 fill:#fff,stroke:#000,stroke-width:1px style S3 fill:#fff,stroke:#000,stroke-width:1px style S4 fill:#fff,stroke:#000,stroke-width:1px style S5 fill:#fff,stroke:#000,stroke-width:1px style S6 fill:#fff,stroke:#000,stroke-width:1px style S7 fill:#fff,stroke:#000,stroke-width:1px style S8 fill:#fff,stroke:#000,stroke-width:1px style x fill:#fff,stroke:#000,stroke-width:1px style y fill:#fff,stroke:#000,stroke-width:1px </pre>												
<p>(57) Abstract</p> <p>A digital filter has an input path and an output path and includes a set of delay elements and a number of taps. The taps couple the input path to the output path. Each of the taps has a coefficient, a multiplier and an adder. Each of the delay elements is disposed between two adjacent taps. The delay elements are placed in either the input path and the output path of the digital filter, such that the digital filter has fewer delay elements in the input path than a direct-form digital filter with the same number of taps in a direct-form structure, and has fewer delay elements in the output path than a transposed-form digital filter with the same number of taps in a transposed-form structure; and such that the digital filter has same transfer function as the direct-form digital filter and the transposed-form digital filter.</p>												

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INTERNATIONAL SEARCH REPORT

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	PCT/US 99/26483

A. CLASSIFICATION OF SUBJECT MATTER					
IPC 7 H03H17/06 H04B3/23 H04B3/32 H04L25/14 H04L25/497 H04L1/00					
According to International Patent Classification (IPC) or to both national classification and IPC					
B. FIELDS SEARCHED					
Minimum documentation searched (classification system followed by classification symbols) IPC 7 H03H H04B H04L					
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched					
Electronic data base consulted during the international search (name of data base and, where practical, search terms used)					
C. DOCUMENTS CONSIDERED TO BE RELEVANT					
Category *	Citation of document, with indication, where appropriate, of the relevant passages				Relevant to claim No.
X	<p>DUNCAN ET AL.: "Strategies for design automation of high speed digital filters" JOURNAL OF VLSI SIGNAL PROCESSING, vol. 9, no. 1/2, September 1995 (1995-09), pages 105-118, XP000525889 Dordrecht, NL page 105, left-hand column, paragraph 1 page 105, right-hand column, paragraph 3 page 108, right-hand column, paragraph 2 - paragraph 4 page 108, right-hand column, paragraph 6 -page 109, left-hand column, paragraph 1 --- -/-</p>				1-20
<input checked="" type="checkbox"/> Further documents are listed in the continuation of box C.			<input checked="" type="checkbox"/> Patent family members are listed in annex.		
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Date of the actual completion of the international search			Date of mailing of the International search report		
26 April 2000			09/05/2000		
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European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016			Scriven, P		

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	PCT/US 99/26483

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
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A	WO 98 43369 A (LEVEL ONE COMMUNICATIONS) 1 October 1998 (1998-10-01) page 7, line 25 - line 28 --- 	1,11

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Information on patent family members

International Application No

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